Experiment No. 02

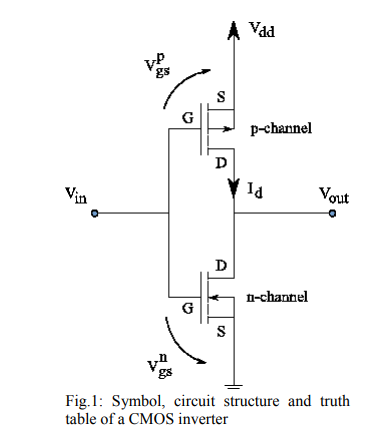
**Schematic of CMOS inverter**

**OBJECTIVE:** To simulate the schematic of the CMOS inverter

**SOFTWARE**: Electric VLSI, LT Spice

**THEORY:**

The inverter is universally accepted as the most basic logic gate doing a Boolean operation on a single input variable. Fig.1 depicts the symbol, truth table and a general structure of a CMOS inverter. As shown, the simple structure consists of a combination of an pMOS transistor at the top and a nMOS transistor at the bottom.

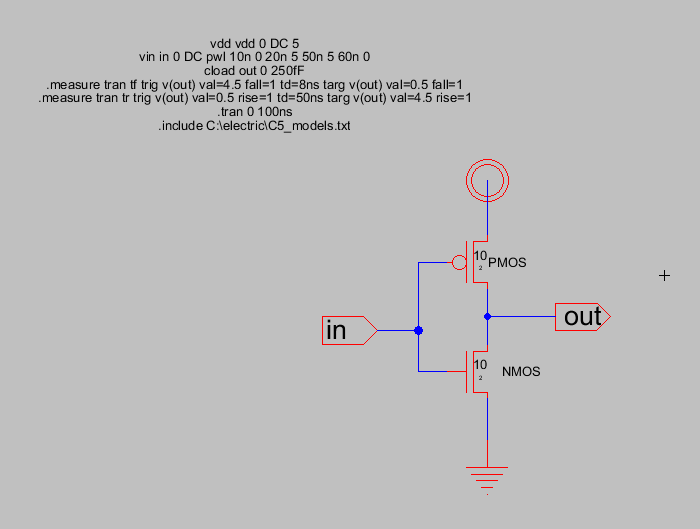


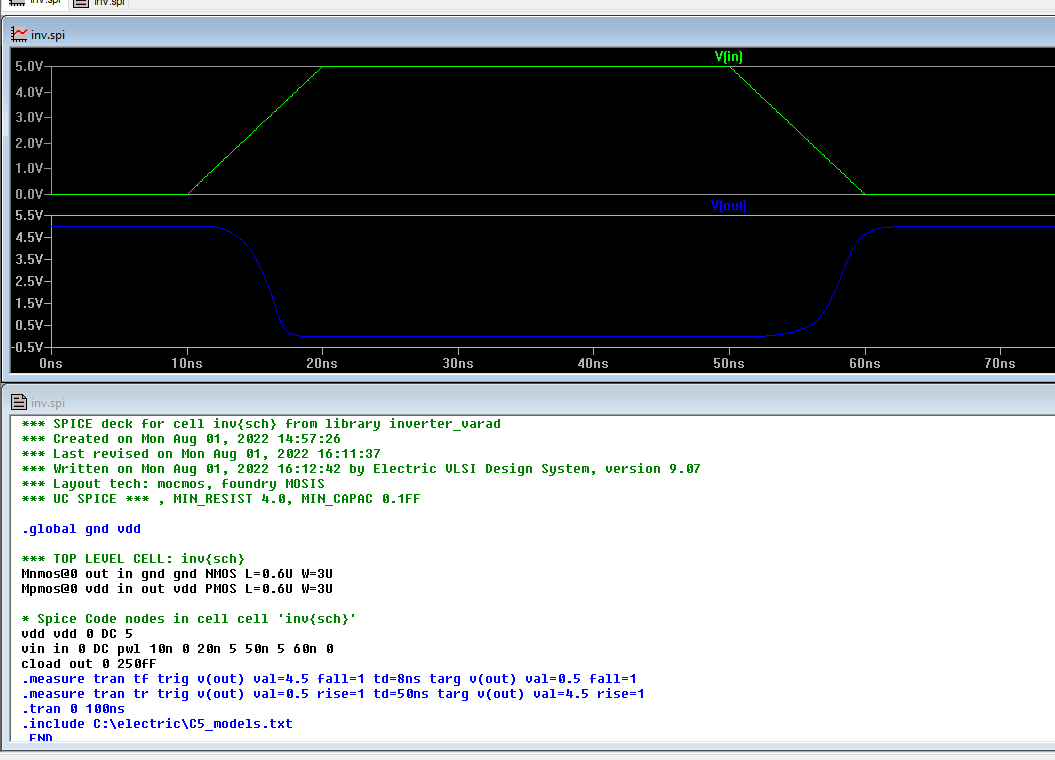
CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor. The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn while the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor transistor logic (TTL) or NMOS logic, which uses all n-channel devices without p-channel devices.

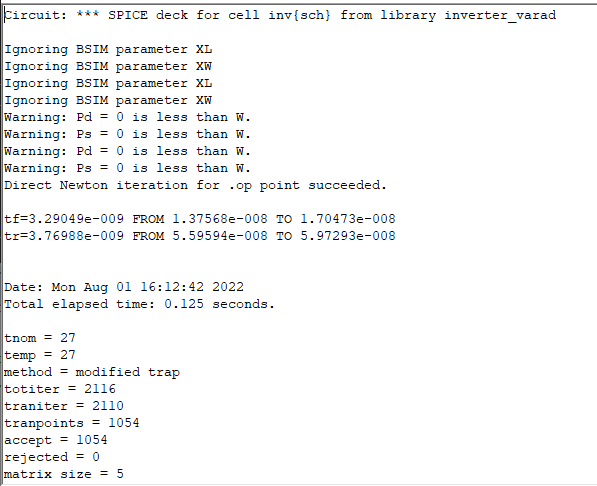
**PROCEDURE:**

1. Open Electric VLSI.
2. In **Files** Menu---click on **new** **library**---Give name to library.
3. In **Edit** Menu---click on **New Cell**---give name to cell---Select view as –schematic.
4. Go to **Components**---Select each required component----do connections.
5. In **Tools** menu---go to **Simulation(spice)**---**Set Spice model**. Select text Spice model and edit it to PMOS or NMOS according to the device.
6. **Create export**s as—in and out.
7. Write Spice code---by clicking on **Misc** in **components** and click on **spice code**.
8. Save library.
9. Simulate the schematic --- in **Tools** menu ----go to **Simulation(spice)**--- click on **Write Spice deck**.
10. LT Spice window gets opened. There Right click on the black window---click on **add trace**.
11. To see fall and rise time--- in **Edit** menu ---click on **SPICE error log**.

**OUTPUT:**







**CONCLUSION:**

**Designing and Simulation of the schematic of the CMOS transistor in electric vlsi was performed successfully. The output of cmos was plotted in ltspice. The delay is shown is spice error log.**